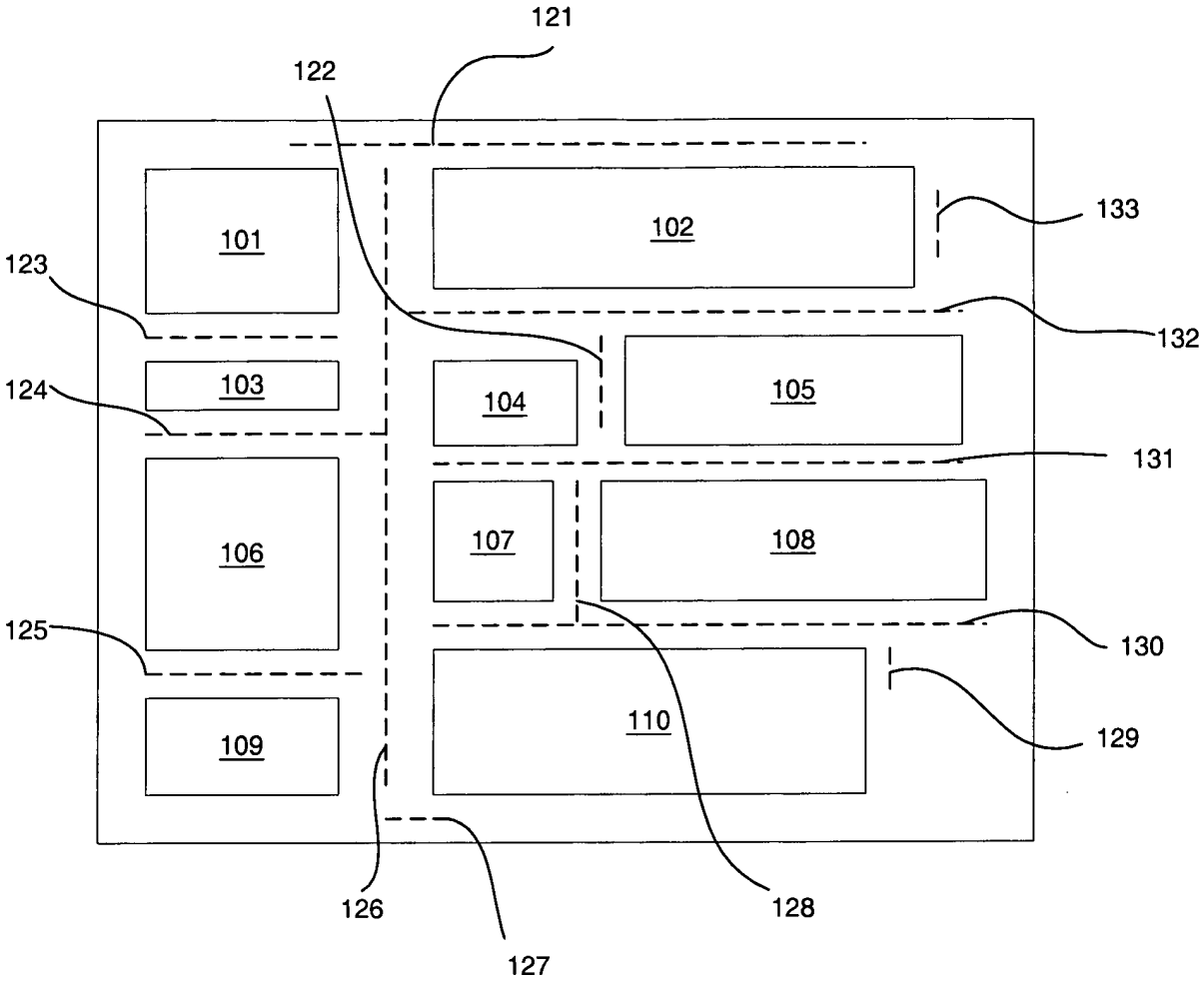


(Prior Art)

Figure 1

Figure 2

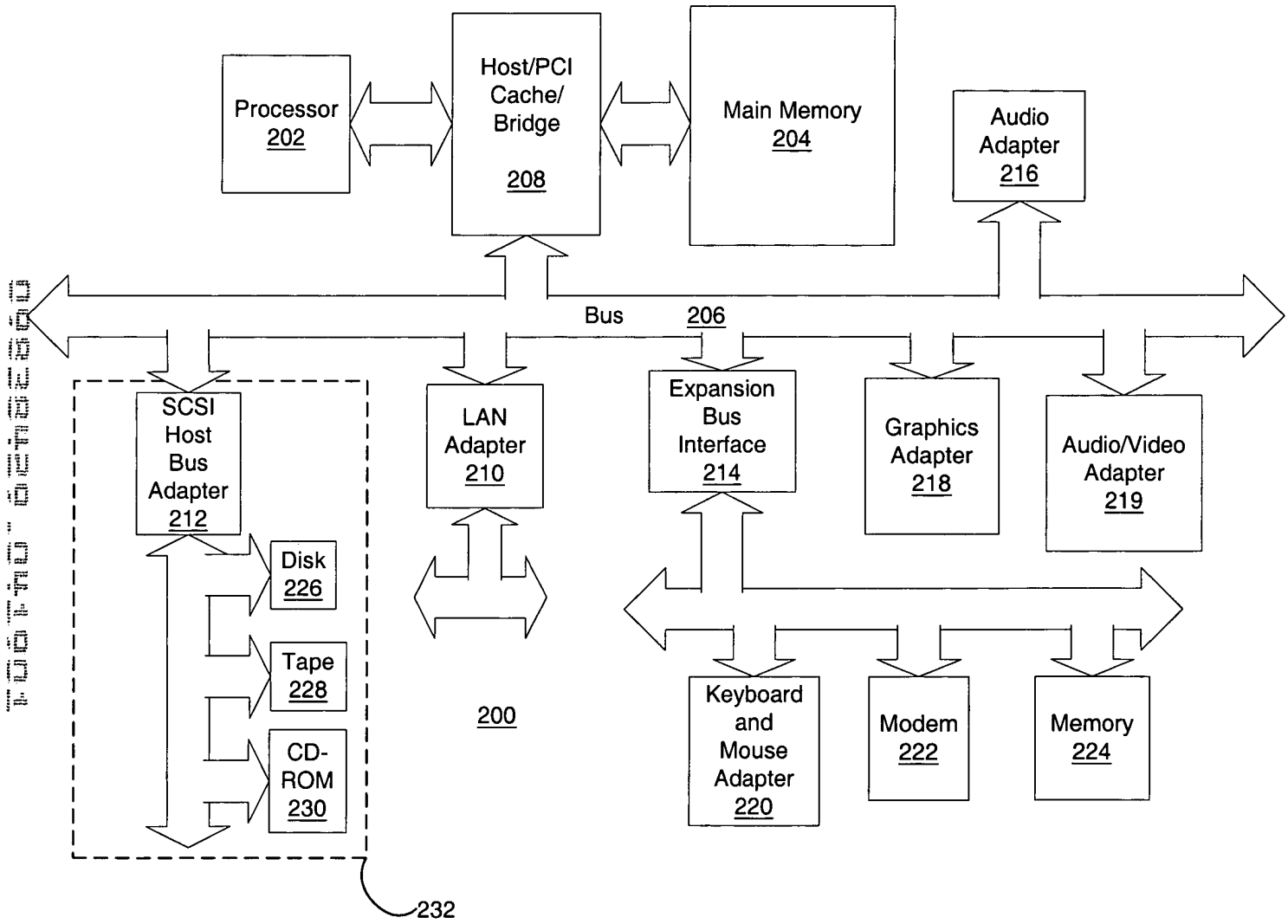

Processor
202
Host/PCI
Cache/
Bridge
208
Main Memory
204
Audio
Adapter
216
Bus 206
SCSI
Host
Bus
Adapter
212
LAN
Adapter
210
Expansion
Bus
Interface
214
Graphics
Adapter
218
Audio/Video
Adapter
219
Disk
226
Tape
228
CD-
ROM
230
200
Keyboard
and
Mouse
Adapter
220
Modem
222
Memory
224
232

Figure 3

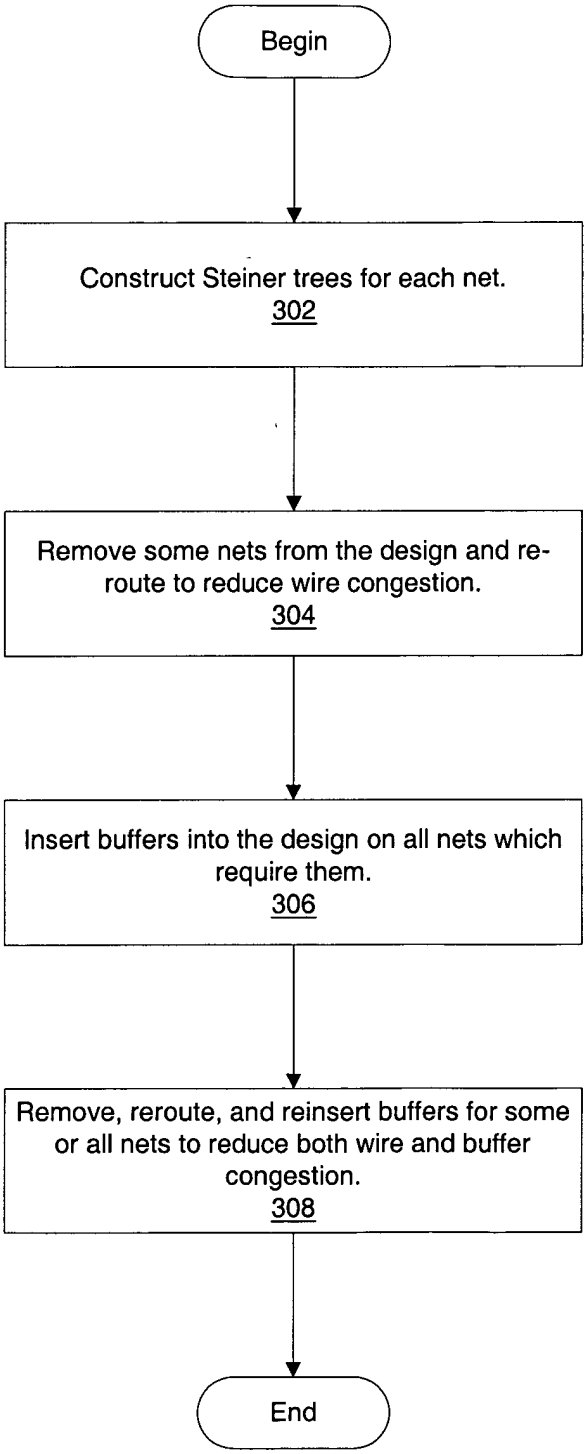
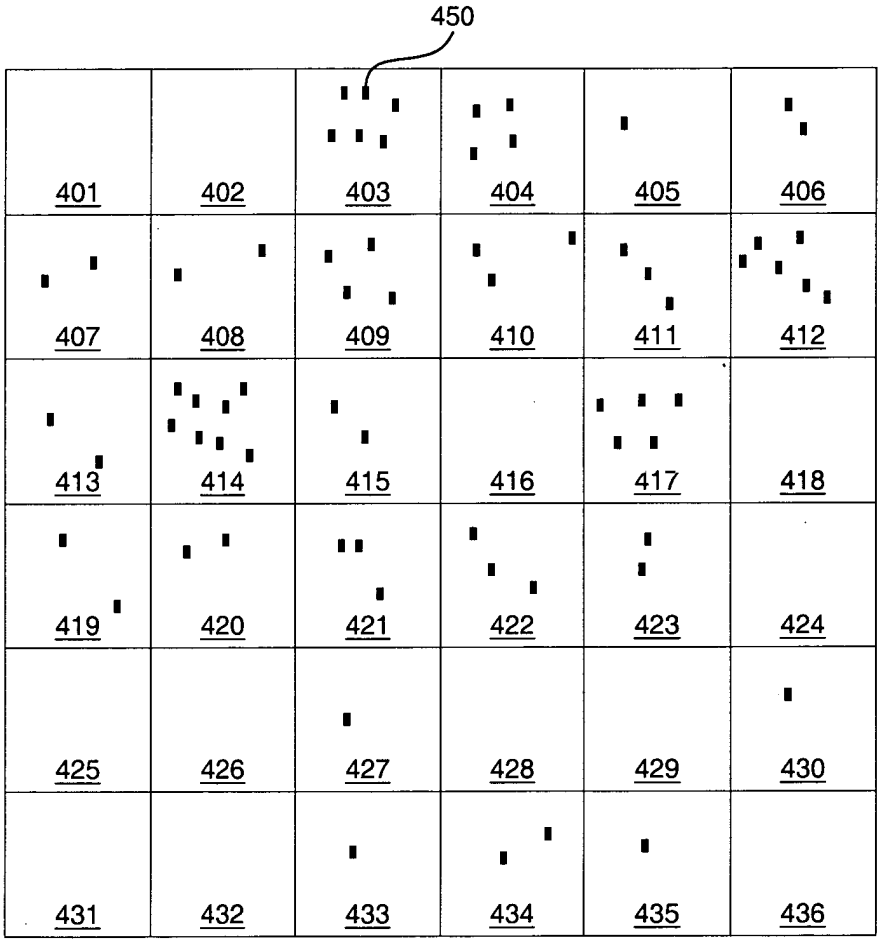

Begin
Construct Steiner trees for each net.
302
Remove some nets from the design and re-route to reduce wire congestion.
304
Insert buffers into the design on all nets which require them.
306
Remove, reroute, and reinsert buffers for some or all nets to reduce both wire and buffer congestion.
308
End

Figure 4A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401
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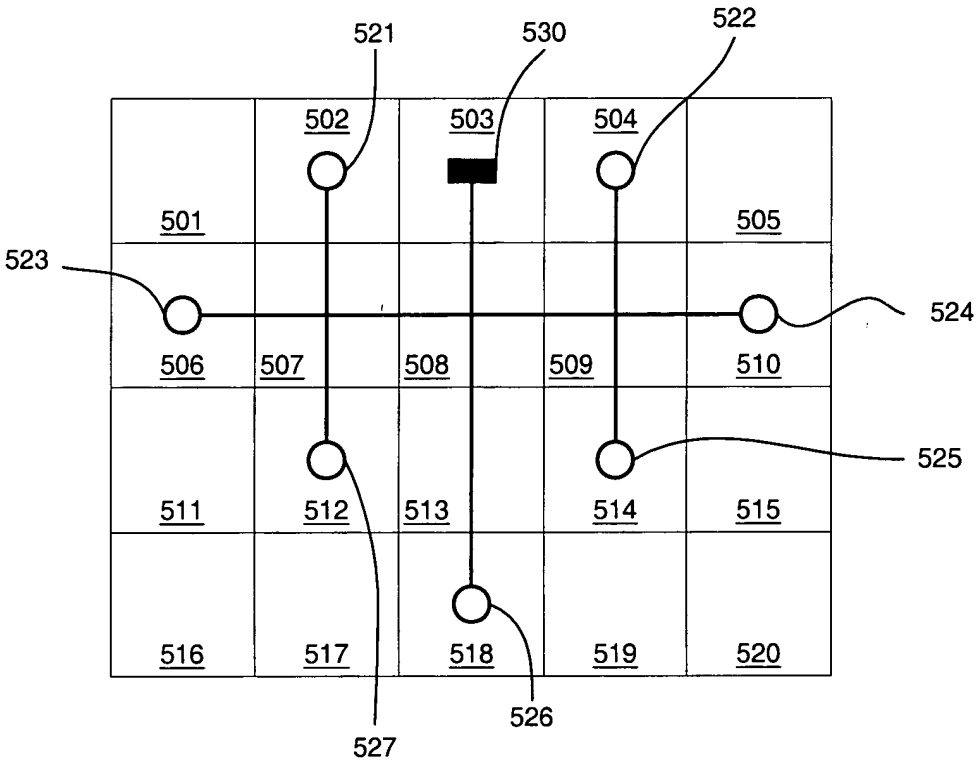
Figure 4B

0 401	0 402	6 403	4 404	1 405	2 406
2 407	2 408	4 409	3 410	3 411	6 412
2 413	8 414	2 415	0 416	5 417	0 418
2 419	2 420	3 421	3 422	2 423	0 424
0 425	0 426	1 427	0 428	0 429	1 430
0 431	0 432	1 433	2 434	1 435	0 436

Figure 5


521
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514
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Figure 6

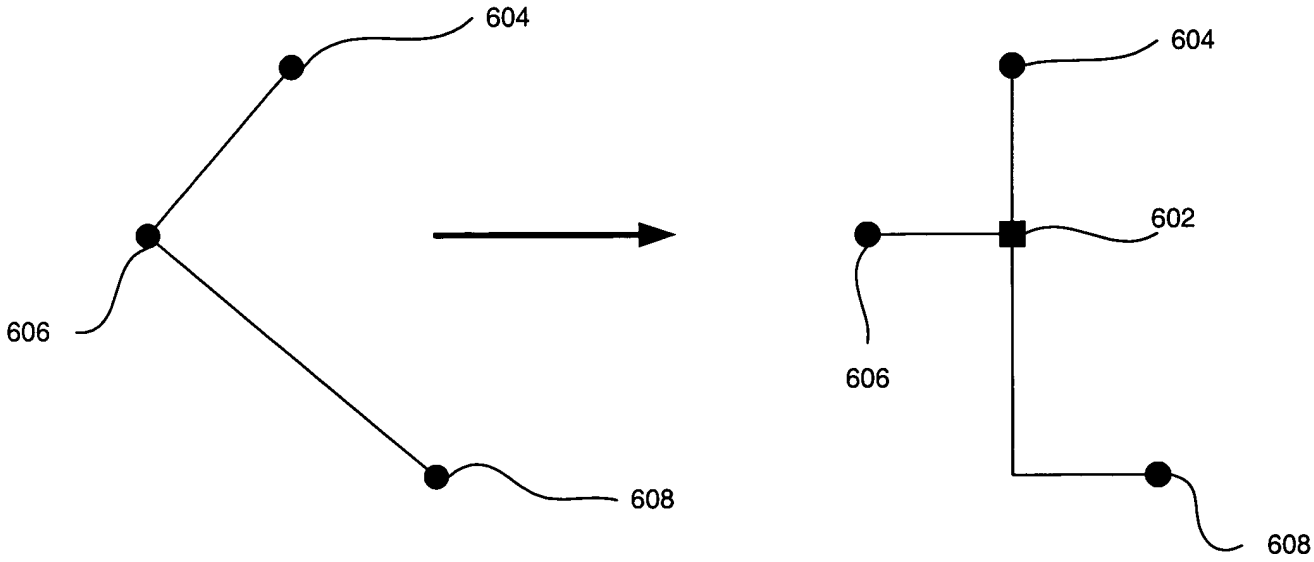
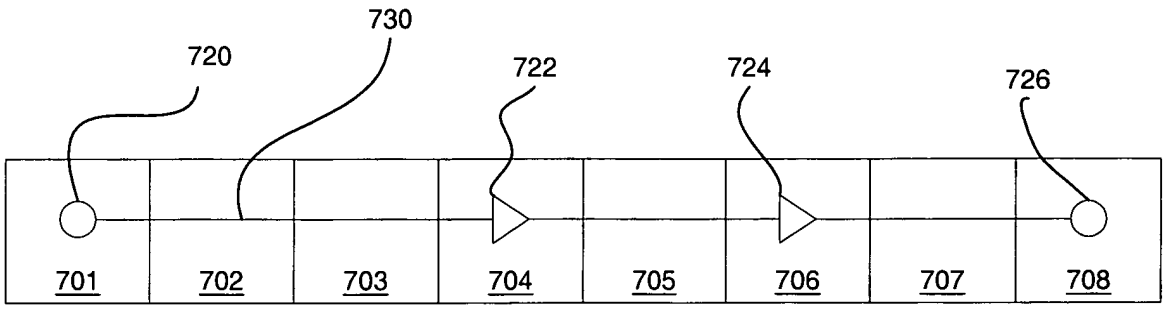


Figure 7



B(v)	8	5	12	3	5	0
b(v)	3	4	2	3	0	0
p(b)	2.5	3.6	2	0.8	4	5
q(v)	1.3	8.6	0.5	∞	1.0	∞

Figure 8

1. Set $C_t[j] = 0$ for $1 \leq j < L_i$ and sink t. Set $v = t$

2. while $v \neq s$ do

   for $j = 1$ to $L_i - 1$ do

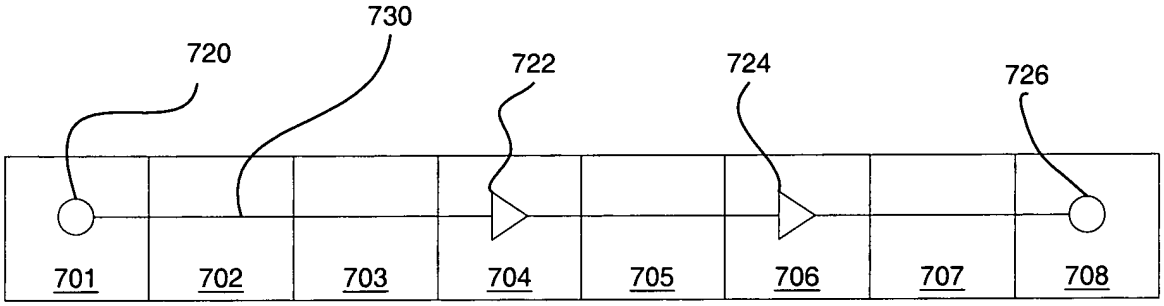
   Set $C_{par(v)}[j] = C_v[j-1]$

   Set $C_{par(v)}[0] = q(par(v)) + min\{C_v[j] \| 0 \leq j < L_i\}$

   Set $v = par(v)$.

3. Let v be such that $par(v) = s$. Return $min\{C_v[j] \| 0 \leq j < L_i\}$.

Figure 9



q(v)	1.3	8.6	0.5	∞	1.0	∞	
$C_v[0]$	2.8	9.6	1.5	∞	1.0	∞	0
$C_v[1]$	9.6	1.5	∞	1.0	∞	0	0
$C_v[2]$	1.5	∞	1.0	∞	0	0	0

900 920 921 922 923 924 925

Figure 10A

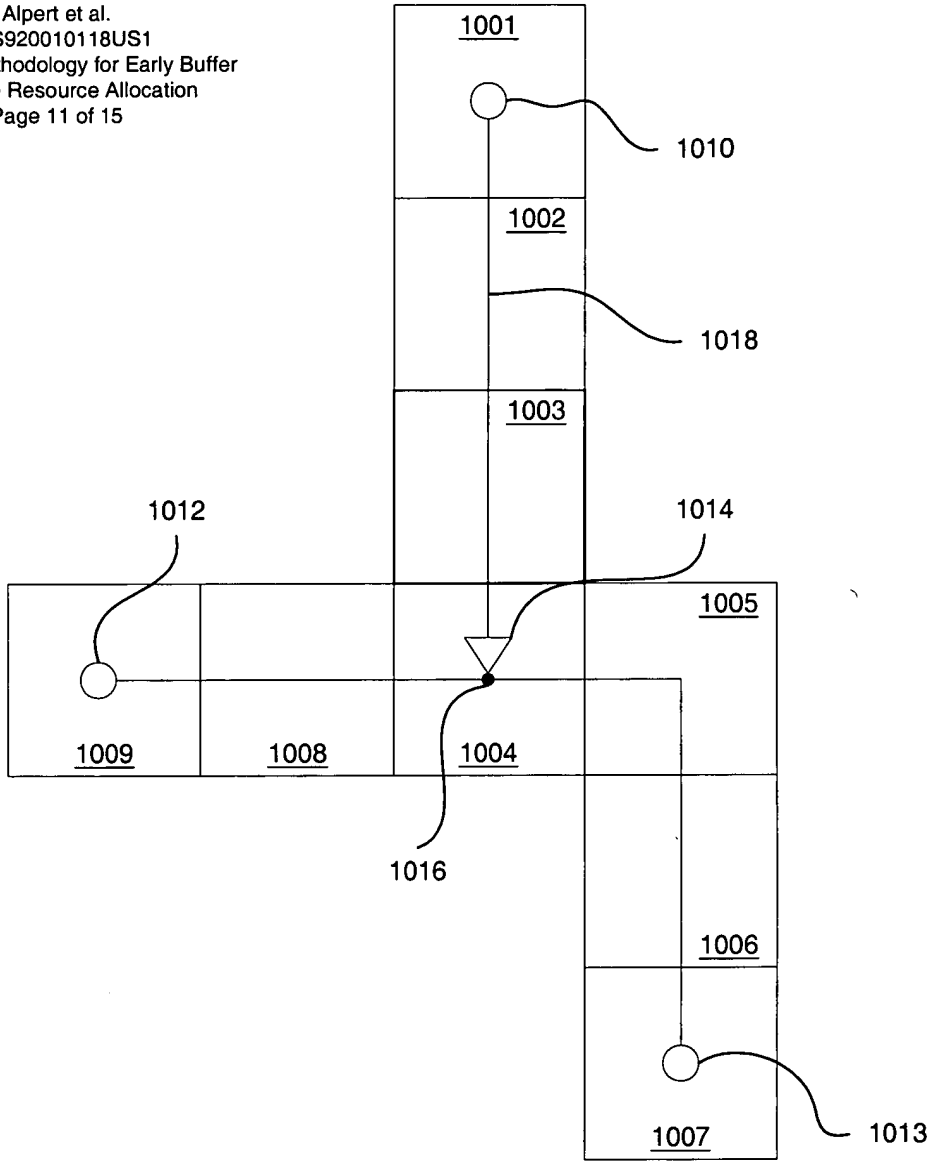

1001
1010
1002
1018
1003
1012
1014
1005
1009
1008
1004
1016
1006
1007
1013

Figure 10B

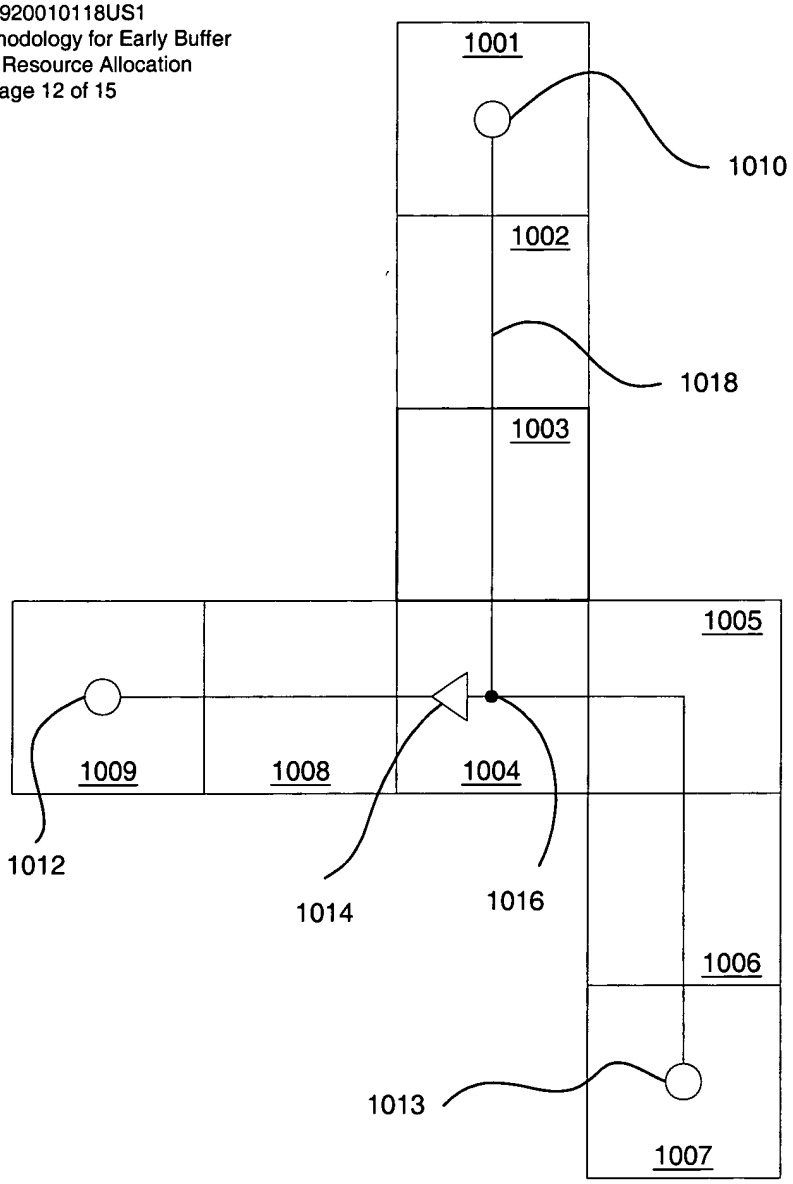


Figure 10C

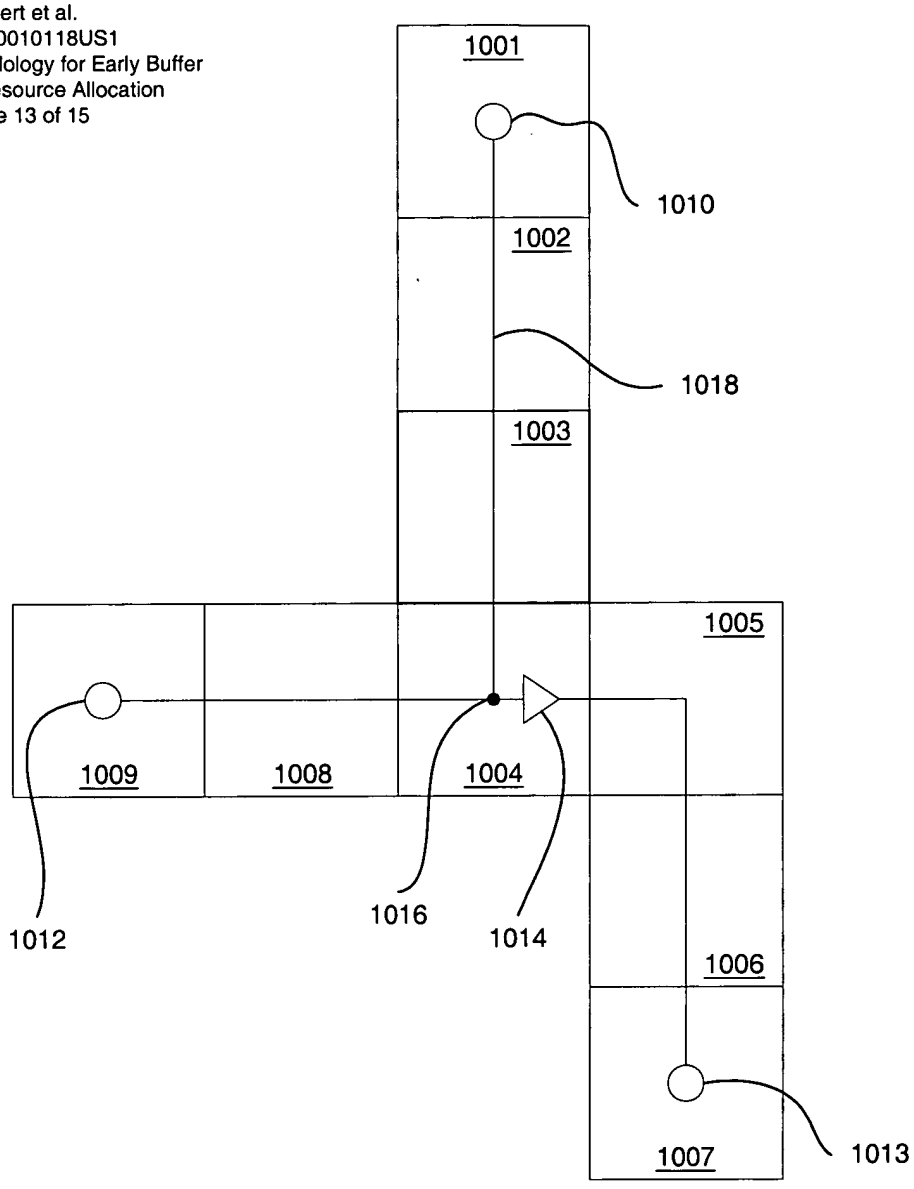

1001
1010
1002
1018
1003
1005
1009
1008
1004
1012
1016
1014
1006
1007
1013

Figure 11

1. Pick an unvisited node v such that all descendants of v have been visited.

   While $v \neq s$ do

2. if v is a sink then
   Set $C_v[j] = 0$ for $1 \leq j < L_i$.

3. if v has one child $l(v)$ then
   for $j = 1$ to $L_i - 1$ do
   Set $C_v[j] = C_{l(v)}[j-1]$
   Set $C_v[0] = q(v) + min\{C_{l(v)}[j] \| 0 \leq j < L_i\}$

4. if v has two children $l(v)$ and $r(v)$ then

4.1 for $j = 2$ to $L_i - 1$ do
   Set $C_v[j] = min\{C_{l(v)}[j_l] + C_{r(v)}[j_r] \| j_l + j_r + 2 = j\}$

4.2 Set $C_v[0] = q(v) + min\{ C_{l(v)}[j_l] + C_{r(v)}[j_r] \| j_l + j_r + 2 \leq L_i\}$

4.3 Set $C_v[1] = \infty$

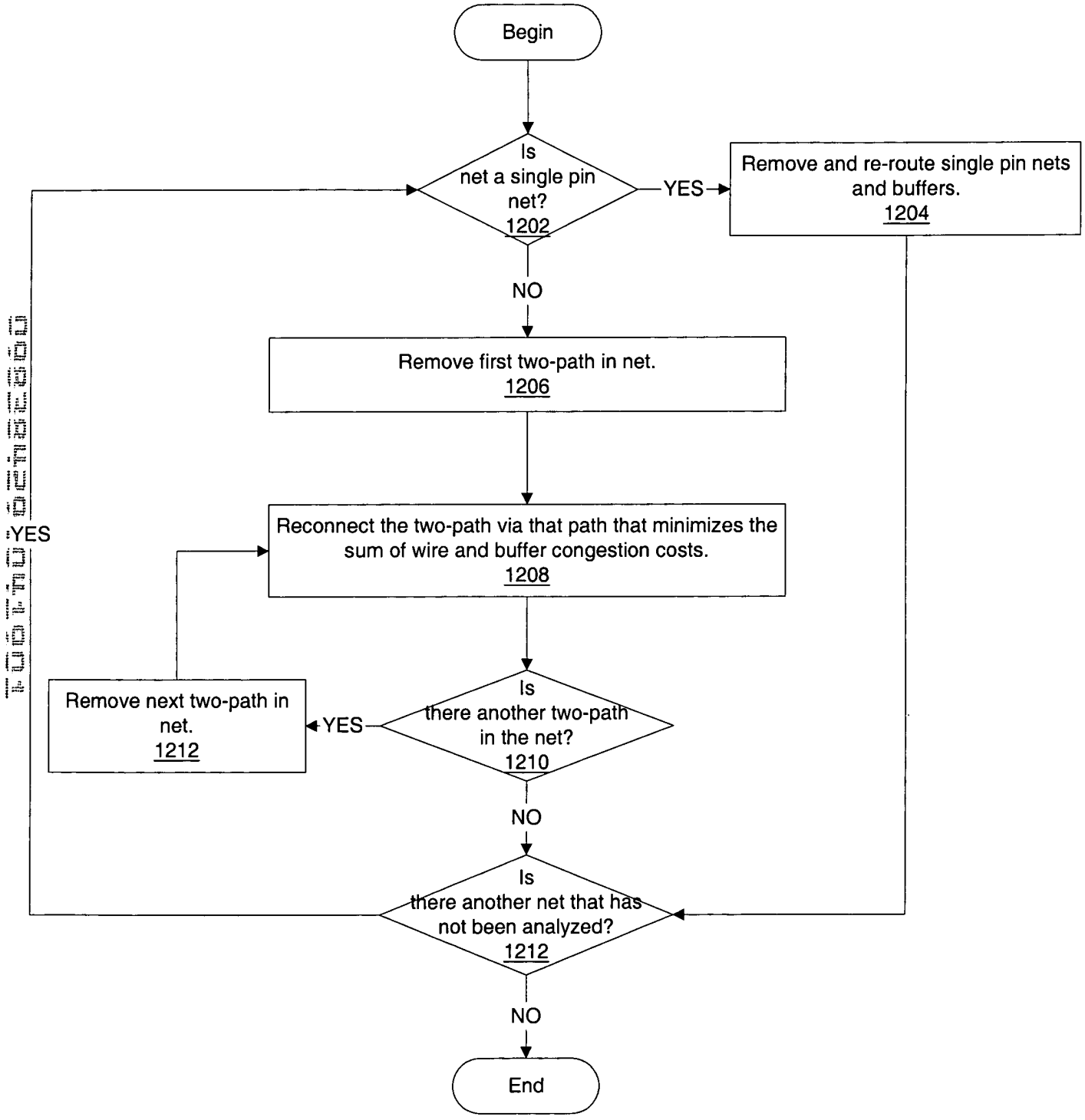
4.4 for $j = 1$ to $L_i - 1$ do
   Set $C_v[j] = min\{C_v[j], q(v) + C_{l(v)}[j-1], q(v) + C_{r(v)}[j-1]\}$

5. mark v as visited
   pick an unvisited node v such that all descendants of v have been visited.

6. Return $min\{C_s[j] \| 0 \leq j < L_i\}$.

1100

Figure 12


Begin
Is net a single pin net? 1202
YES
Remove and re-route single pin nets and buffers. 1204
NO
Remove first two-path in net. 1206
Reconnect the two-path via that path that minimizes the sum of wire and buffer congestion costs. 1208
Is there another two-path in the net? 1210
YES
Remove next two-path in net. 1212
NO
Is there another net that has not been analyzed? 1212
YES
NO
End